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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,731	SONG, LEILEI	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-10,25 and 26* is/are rejected.

7)☒ Claim(s) *5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 1-10, 25 and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 25 and 26 recite "wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode". Nowhere in the specification does the Applicant teach "wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode" and in particular, the Applicant never mentions "operating mode" much less "normal operating mode" anywhere in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-10, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 25 and 26 recite "wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode".

The term "relative to" in is a relative term which renders the claims indefinite. The term "relative to" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claims 1, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. Claims 1, 25 and 26 recite "wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode". The omitted elements are: the relationship between "given interval of time" and "normal operating mode". The omitted elements are: the relationship between "reduced power mode" and "given interval of time".

Response to Arguments

3. Applicant's arguments filed 12/22/2005 have been fully considered but they are not persuasive.

The Examiner begins by summarizing the previous rejection of claims 1, 25 and 16 for the Applicant's convenience:

Noguchi teaches determining if an actual number of errors is less than a maximum error correction capability (Figure 2 in Noguchi teaches determining if uncorrectable errors exist and flagging the uncorrectable errors with flags, UNC(A1), UNC(B1), UNC(A2) & UNC(B2), i.e., if UNC(A1)=0 there are no uncorrectable errors with respect to the A1 decoding and the actual numbers are below the maximum error correction capability of the A1 decoding, if UNC(B1)=0 there are no uncorrectable errors with respect to the B1 decoding and the actual numbers are below the maximum error correction capability of the B1 decoding, if UNC(A2)=0 there are no uncorrectable errors with respect to the A2 decoding and the actual numbers are below the maximum error correction capability of the A2 decoding & if UNC(B2)=0 there are no uncorrectable errors with respect to the B2 decoding and the actual numbers are below the maximum error correction capability of the B2 decoding); and performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (Step S3 in Figure 2 of Noguchi teaches that when UNC(A1)=0, i.e., the actual numbers are below the maximum error correction capability of the A1 decoding correction is terminated; Note: the abstract in Noguchi teaches that error correction is terminated to reduce power consumption; hence Noguchi teaches performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability, that is; when UNC(A1)=0; **Note also that Figure 2 in Noguchi is an error correction algorithm for an error correction process and that the termination routine taught in Noguchi is incorporated into the error correction**

process as a part of the error correction process that is the error correction process taught in Noguchi *is* a reduced power error correction process whereby error correction is explicitly performed in a reduced power mode in the decoder of the error correction system used for implementing the reduced power error correction process taught in Noguchi when the actual number of errors is less than the maximum error correction capability), wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode (Figure 1 in Noguchi is a data correction device capable of terminating operations to conserve power when error correction is not needed, Data Error Correction Device 20 receives input data codewords to determine error locations and error values of erroneous data codewords that are provided to a data processing device for the purposes of correcting and decoding erroneous data codewords and does not implement any type of error correction or decoding of data codewords itself; that is, nowhere does Noguchi teach any output from the Data Error Correction Device 20 that would alter the timing or clocking of any other device so one can only assume that codewords are processed and decoded in another device separate from the Data Error Correction Device 20 without altering the normal timing of the decoding process in any other device necessary for error correction; Noguchi only teaches a means for saving power in on component, the Data Error Correction Device 20 in Figure 1 of Noguchi, and does not teach anywhere in the Noguchi patent the alteration of normal timing in any other device associated with error correction).

The Applicant contends, "Noguchi does not disclose or suggest wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode, as required by independent claims 1, 25, and 26, as amended".

The Examiner disagrees and asserts that Noguchi teaches performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (Step S3 in Figure 2 of Noguchi teaches that when UNC(A1)=0, i.e., the actual numbers are below the maximum error correction capability of the A1 decoding correction is terminated; Note: the abstract in Noguchi teaches that error correction is terminated to reduce power consumption; hence Noguchi teaches performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability, that is; when UNC(A1)=0; **Note also that Figure 2 in Noguchi is an error correction algorithm for an error correction process and that the termination routine taught in Noguchi is incorporated into the error correction process as a part of the error correction process that is the error correction process taught in Noguchi *is* a reduced power error correction process whereby error correction is explicitly performed in a reduced power mode in the decoder of the error correction system used for implementing the reduced power error correction process taught in Noguchi when the actual number of errors is less than the maximum error correction capability**), wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode (Figure 1 in Noguchi is a data correction device capable of

terminating operations to conserve power when error correction is not needed, Data Error Correction Device 20 receives input data codewords to determine error locations and error values of erroneous data codewords that are provided to a data processing device for the purposes of correcting and decoding erroneous data codewords and does not implement any type of error correction or decoding of data codewords itself; that is, nowhere does Noguchi teach any output from the Data Error Correction Device 20 that would alter the timing or clocking of any other device so one can only assume that codewords are processed and decoded in another device separate from the Data Error Correction Device 20 without altering the normal timing of the decoding process in any other device necessary for error correction; Noguchi only teaches a means for saving power in on component, the Data Error Correction Device 20 in Figure 1 of Noguchi, and does not teach anywhere in the Noguchi patent the alteration of normal timing in any other device associated with error correction).

The Applicant contends, "Noguchi and Cameron, alone or in combination, do not disclose or suggest providing a plurality of intermediate polynomials, and wherein the step of reducing power consumption in the error correction system when the actual number of errors is less than the maximum error correction capability further comprises the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree, as required by claim 3".

The Examiner disagrees and asserts that the Abstract in Cameron teaches that the test for uncorrectable errors comprises determining if the degree of the Error Locator

Polynomial $\Lambda(x)$ and the degree of the Error Magnitude Polynomial $\Omega(x)$ are less than predetermined values. One of ordinary skill in the art at the time the invention was made would have known that the Error Locator Polynomial $\Lambda(x)$ and the degree of the Error Magnitude Polynomial $\Omega(x)$ are intermediate polynomials and uncorrectable errors are a result of exceeding the maximum error correction capability of a code.

The Applicant contends that Noguchi and Cameron, alone or in combination, do not disclose or suggest "wherein one intermediate polynomial is a first error evaluator polynomial R(x), wherein one intermediate polynomial is a first error locator polynomial F(x), wherein $R^{(r+1)}(x) = F^{(r+1)}(x) \bullet S(x) \bmod x^{2t}$ wherein r is a number of iterations, S(x) is a syndrome polynomial, and t is a number of errors capable of being corrected, wherein one intermediate polynomial is a second error evaluator polynomial Q(x), wherein one intermediate polynomial is a second error locator polynomial G(x), wherein $Q^{(r+1)}(x) = G^{(r+1)}(x) \bullet S(x) \bmod x^{2t}$, wherein the step of determining if a degree of at least one of the intermediate polynomials is less than a predetermined degree further comprises the step of determining if a degree of either R(x) or Q(x) is less than a predetermined degree, wherein R(x) and F(x) are valid when a degree of R(x) is less than the predetermined degree, and wherein Q(x) and G(x) are valid when a degree of Q(x) is less than the predetermined degree, as required by claim 4".

The Examiner disagrees and asserts that even the Applicant acknowledges on page 11 of the Applicant's disclosure that the equations in claim 4 are equations specified by the

Modified Euclidean Algorithm. The Modified Euclidean Algorithm is not the Applicant's invention just as the equations of claim 4 are not the Applicant's invention.

The Applicant contends, "Noguchi and Cameron, alone or in combination, do not disclose or suggest determining a plurality of syndromes; determining if all of the syndromes have a predetermined value; and reducing power consumption of the decoder of the error correction system when all of the syndromes have the predetermined value, as required by claim 7".

The Examiner disagrees and asserts that Figure 2 in Noguchi teaches that whenever SYN(B1)=0 and UNC(A1)=0, correction is terminated thereby reducing power. Note: one of ordinary skill in the art at the time the invention was made that SYN(B1) can only equal zero when all of the syndromes of the codeword B1 equal the predetermined value of zero.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 7, 8, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticiapted by Noguchi; Nobuaki (US 6611939 B1).

35 U.S.C. 102(e) rejection of claims 1, 25 and 26.

Noguchi teaches determining if an actual number of errors is less than a maximum error correction capability (Figure 2 in Noguchi teaches determining if uncorrectable errors exist and flagging the uncorrectable errors with flags, UNC(A1), UNC(B1), UNC(A2) & UNC(B2), i.e., if UNC(A1)=0 there are no uncorrectable errors with respect to the A1 decoding and the actual numbers are below the maximum error correction capability of the A1 decoding, if UNC(B1)=0 there are no uncorrectable errors with respect to the B1 decoding and the actual numbers are below the maximum error correction capability of the B1 decoding, if UNC(A2)=0 there are no uncorrectable errors with respect to the A2 decoding and the actual numbers are below the maximum error correction capability of the A2 decoding & if UNC(B2)=0 there are no uncorrectable errors with respect to the B2 decoding and the actual numbers are below the maximum error correction capability of the B2 decoding); and performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability (Step S3 in Figure 2 of Noguchi teaches that when UNC(A1)=0, i.e., the actual numbers are below the maximum error correction capability of the A1 decoding correction is terminated; Note: the abstract in Noguchi teaches that error correction is terminated to reduce power consumption; hence Noguchi teaches performing error correction in a reduced power mode in a decoder of the error

correction system when the actual number of errors is less than the maximum error correction capability, that is; when UNC(A1)=0; **Note also that Figure 2 in Noguchi is an error correction algorithm for an error correction process and that the termination routine taught in Noguchi is incorporated into the error correction process as a part of the error correction process that is the error correction process taught in Noguchi *is* a reduced power error correction process whereby error correction is explicitly performed in a reduced power mode in the decoder of the error correction system used for implementing the reduced power error correction process taught in Noguchi when the actual number of errors is less than the maximum error correction capability**), wherein said reduced power mode consumes less power in a given interval of time relative to a normal operating mode (Figure 1 in Noguchi is a data correction device capable of terminating operations to conserve power when error correction is not needed, Data Error Correction Device 20 receives input data codewords to determine error locations and error values of erroneous data codewords that are provided to a data processing device for the purposes of correcting and decoding erroneous data codewords and does not implement any type of error correction or decoding of data codewords itself; that is, nowhere does Noguchi teach any output from the Data Error Correction Device 20 that would alter the timing or clocking of any other device so one can only assume that codewords are processed and decoded in another device separate from the Data Error Correction Device 20 without altering the normal timing of the decoding process in any other device necessary for error correction; Noguchi only teaches a means for saving

power in on component, the Data Error Correction Device 20 in Figure 1 of Noguchi, and does not teach anywhere in the Noguchi patent the alteration of normal timing in any other device associated with error correction).

35 U.S.C. 102(e) rejection of claim 2.

See col. 10, lines 36-44 in Noguchi. Note: The Authoritative Dictionary of IEEE Standards Terms defines gating as the application of inhibiting pulses during part of a cycle of equipment operation; hence stopping a clock as taught in col. 10, lines 36-44 of Noguchi is a means for gating.

35 U.S.C. 102(e) rejection of claims 7 and 8.

Col. 7, lines 1-5 in Noguchi teaches that SYN(A1), SYN(B1), SYN(A2) & SYN(B2) are flags and are set to 0 if all the syndromes for the respective decodings are zero. Syndrome calculation means 11 in Figure 1 of Noguchi is a means for determining a number of syndromes. Flagging the B1 decoding using the SYN(B1) flag is a means for determining if all the syndromes have the predetermined value of zero or not. Figure 2 in Noguchi teaches that whenever SYN(B1)=0 and UNC(A1)=0, correction is terminated thereby reducing power. **Note: one of ordinary skill in the art at the time the invention was made that SYN(B1) can only equal zero when all of the syndromes of the codeword B1 equal the predetermined value of zero.**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 3, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi; Nobuaki (US 6611939 B1) in view of Cameron; Kelly (US 5099482 A).

35 U.S.C. 103(a) rejection of claims 3 and 9.

Noguchi substantially teaches the claimed invention described in claims 1, 2, 7 and 8 (as rejected above).

However Noguchi does not explicitly teach the specific use of the particular elements of a decoder for Reed-Solomon codes nor does Noguchi teach how an uncorrectable error is determined.

Cameron, in an analogous art, teaches use of the particular elements of a decoder for Reed-Solomon codes and how an uncorrectable error is determined from intermediate

polynomials (Note: the Abstract in Cameron teaches that the test for uncorrectable errors comprises determining if the degree of the Error Locator Polynomial $\Lambda(x)$ and the degree of the Error Magnitude Polynomial $A(x)$ are less than predetermined values).

Note: Noguchi teaches general syndrome based error correction codes, which include Reed-Solomon codes whereas Cameron explicitly focuses on a specific type of syndrome based code, i.e., Reed-Solomon codes. Note: one of ordinary skill in the art at the time the invention was made would have been highly motivated to use a Reed-Solomon code since Reed-Solomon codes form the core of the most powerful known algebraic codes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Noguchi with the teachings of Cameron by including use of the particular elements of a decoder for Reed-Solomon codes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the particular elements of a decoder for Reed-Solomon codes would have provided the opportunity for using one of the most powerful known algebraic codes.

35 U.S.C. 103(a) rejection of claim 10.

If the Syndromes are not all zero, error correction circuitry is enabled to correct errors. Calculating error polynomials is a required step for decoding Reed-Solomon codes.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi; Nobuaki (US 6611939 B1) and Cameron; Kelly (US 5099482 A) in view of Oh; Kyu-taeg et al. (US 6256763 B1, hereafter referred to as Oh).

35 U.S.C. 103(a) rejection of claim 4.

Noguchi and Cameron substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Noguchi and Cameron do not explicitly teach the specific use of the modified Euclidean Algorithm.

Oh, in an analogous art, teaches use of the modified Euclidean Algorithm (Figure 1 in Oh).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Noguchi and Cameron with the teachings of Oh by including use of the modified Euclidean Algorithm. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the modified Euclidean Algorithm would have provided power consumption reduction and complexity reduction aspects.

Allowable Subject Matter

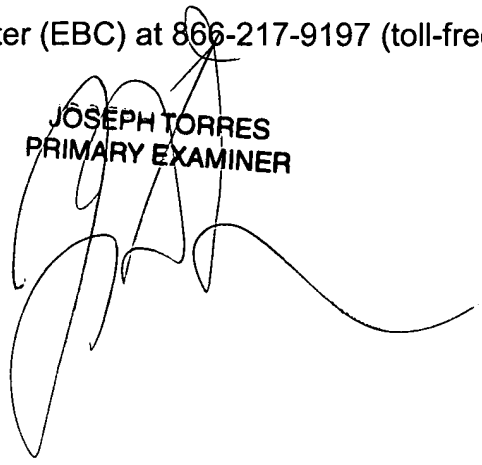
7. Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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